CLAIMS

1. A programmable memory cell useful in a memory array having column bitlines and row wordlines, the memory cell comprising:

a transistor having a gate, a gate dielectric between the gate and over a substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region therebetween and under said gate, the gate being formed from one of said column bitlines; and

wherein the second doped semiconductor region of the transistor is connected to one of said row wordlines, wherein said row wordlines are formed from a buried N+ layer.

2. The memory cell of Claim 1 wherein the gate dielectric of the transistor is thicker proximal to the first and second doped semiconductor regions than at said channel region.

3. The memory cell of Claim 1 wherein the gate and said second doped semiconductor region is laterally separated by a distance D.

4. The memory cell of Claim 3 wherein said distance D is sufficient to prevent a short circuit with said first or second doped semiconductor regions.

5. A method of operating a programmable memory array comprising a plurality of row wordlines, a plurality of column bitlines, and a plurality of memory cells at respective

crosspoints of the row lines and column lines, said memory cells comprising a transistor having a gate, a gate dielectric between the gate and over a substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region therebetween and under said gate, the gate being formed from one of said column bitlines, and the second doped semiconductor region of the transistor connected to one of said row wordlines, said row wordlines being formed from a buried n+ layer, the method comprising:

applying a first voltage to a selected one of the column bitlines and gate of a selected transistor; and

applying a second voltage to a selected one of the row wordlines;

wherein the first voltage and the second voltage form a potential difference across the gate dielectric of said selected transistor to cause the formation of a programmed doped region in said substrate in said channel region of said selected transistor.

6. The method of Claim 5 wherein said selected transistor is read by applying a fourth voltage on the gate of said selected transistor and monitoring for a current flowing from said gate to said selected column bitline.

7. A programmable memory array comprising a plurality of row wordlines, a plurality of column bitlines, and a plurality of memory cells at respective crosspoints of the row wordlines and column bitlines, each of the memory cells comprising:

a transistor having a gate, a gate dielectric between the gate and over a substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region therebetween and under said gate, the gate being formed from one of said column bitlines; and

wherein the second doped semiconductor region of the transistor is connected to one of said row wordlines, wherein said row wordlines are formed from a buried N+ layer.

8. The memory array of Claim 7 wherein said column bitlines are connected to said gate by a column bitline segment.

9. The memory array of Claim 7 wherein the gates of said transistors do not overlap either of said first and second n+ doped semiconductor regions of said respective transistor.

10. The memory array of Claim 8 wherein the gate dielectric of the transistors are thicker proximal to the respective first and second doped semiconductor regions than at said channel region.

11. The memory array of Claim 8 wherein said transistors have their gate and said second doped semiconductor region is laterally separated by a distance D.

12. The memory array of Claim 11 wherein said distance D is sufficient to prevent a short circuit from the gate to said first or second doped semiconductor regions.

13. The memory array of Claim 18 wherein said memory cells further including a programmed doped region formed in said substrate in said channel region when said memory cell has been programmed.

14. A programmable memory cell useful in a memory array having column bitlines and row wordlines, the memory cell comprising:

a transistor having a gate, a gate dielectric between the gate and over a substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region therebetween and under said gate, the gate being formed from one of said column bitlines; and

wherein the second doped semiconductor region of the transistor is connected to one of said row wordlines, wherein said row wordlines are formed from a buried P+ layer.

15. The memory cell of Claim 14 wherein the gate dielectric of the transistor is thicker proximal to the first and second doped semiconductor regions than at said channel region.

16. The memory cell of Claim 14 wherein the gate and said second doped semiconductor region is laterally separated by a distance D.

17. The memory cell of Claim 16 wherein said distance D is sufficient to prevent a short circuit with said first or second doped semiconductor regions.

18. A method of operating a programmable memory array comprising a plurality of row wordlines, a plurality of column bitlines, and a plurality of memory cells at respective crosspoints of the row lines and column lines, said memory cells comprising a transistor having a gate, a gate dielectric between the gate and over a substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region therebetween and under said gate, the gate being formed from one of said column bitlines, and the second doped semiconductor region of the transistor connected to one of said row wordlines, said row wordlines being formed from a buried p+ layer, the method comprising:

applying a first voltage to a selected one of the column bitlines and gate of a selected transistor; and

applying a second voltage to a selected one of the row wordlines;

wherein the first voltage and the second voltage form a potential difference across the gate dielectric of said selected transistor to cause the formation of a programmed doped region in said substrate in said channel region of said selected transistor.

19. The method of Claim 18 wherein said selected transistor is read by applying a fourth voltage on the gate of said selected transistor and monitoring for a current flowing from said gate to said selected column bitline.